REMARKS

Claims 1 – 11 remain in the application and stand finally rejected. The final rejection is respectfully traversed.

Patentability under 35 USC §101

Claim 9 is finally rejected under 35 USC §101 for being directed to non-statutory subject matter. Specifically, the final Office action asserts that "[c]laim 9 is directed to a computer program. For claim 9 to be statutory, the applicant must state 'A computer readable medium storing a computer program' (or equivalent) not a computer program comprising a computer readable medium."

However, that is not what claim 9 recites. Claim 9 recites a "computer program **product** comprising a **computer readable medium** with program **instructions stored thereon** and effective when executed by a computer system to cause the computer system" at lines 1 – 3 (emphasis added). Therefore, claim 9 is statutory. Reconsideration and withdrawal of the final rejection of claim 9 under 35 U.S.C. §101 is respectfully requested.

Patentability under 35 USC §112

Claims 10 and 11 are finally rejected under 35 USC §112 for failing the written description requirement. Specifically, the final Office action asserts that the specification, as filed, would not convey to a skilled artisan that the "sequencer [remains] unchanged by additions and removals of connected and disconnected said raster image processors." Thus, the final Office action further asserts that "[t]his limitation is not described in the applicants specification." The final Office action responds to the applicant's prior remarks, asserting that "Applicant's argument that the sequencer does

not require changing does not equate to the sequencer remaining unchanged. At the very least, the sequencer will become changed by the number of raster image processors connected. Further, adding/removing nodes to a network does change other nodes in that connections are now available to the nodes." This argument is specious.

First of all, while the adding raster image processors may change the number of nodes the network[1], it does not follow that connecting raster image processors to the network changes the sequencer connected to the same network. For example, attaching computers to a network, e.g., a wired Ethernet 100BASE-T or by WiFi, does not change other connected computers. Does connecting ones' computer to the Internet change other computers connected to the Internet? No! Does disconnecting an Internet Service Provider (ISP, e.g., AOL), from the Internet change other computers connected to the Internet through other ISPs? No! Therefore, "adding/removing nodes to a network does [not] change other nodes" and connecting and disconnecting raster image processors to/from the network does not change the sequencer connected to the same network. Therefore also, the sequencer remaining unchanged by additions and removals of connected and disconnected raster image processors is supported by the application as filed.

Furthermore, there is nothing of record to support the assertion that "adding/removing nodes to a network does change other nodes in that connections are now available to the nodes." It is, therefore, apparent from the above conclusion of obviousness, that Official Notice[2] is being relied upon to teach this. "It would not be appropriate for the examiner to take official notice of facts without citing a prior art

[1] See, claim 1, lines 9 – 11 (i.e., the "sequencer … has an output port networked and communicating with, and directly connected to, the input ports of said plurality of raster image processors and an input port receiving a print data stream").
[2] *See*, MPEP §2144.03.

reference where the facts asserted to be well known are not capable of instant and unquestionable demonstration as being well-known.[3]"

"[I]n the absence of any demand by appellant for the examiner to produce authority for his statement, we will not consider this contention.[4]" Applicant hereby so demands. Further, as previously noted, the applicants can provide extrinsic evidence showing that a skilled artisan could indeed understand from the specification that the "sequencer [remains] unchanged by additions and removals of connected and disconnected said raster image processors." Upon production of authority to support this assertion of Official Notice, the applicant will provide such extrinsic evidence. Accordingly, believing to have shown the recitations of claims 10 and 11 to be supported by the present application as filed and specifically by Figure 2 and any appurtenant description thereof, reconsideration[5] and withdrawal of the final rejection of claims 10 and 11 under 35 U.S.C. §112 is respectfully requested.

Patentability under 35 USC §103

Claims 1 and 3 are finally rejected under 35 USC §103(a) as being unpatentable over U.S. Patent No. 6,825,943 to Barry et al. in view of U.S. Patent No. 6,315,390 to Fujii. Claims 2 and 6 – 11 are finally rejected under 35 USC §103(a) as being unpatentable over Barry et al. and Fujii in further view of U.S. Patent No. 6,532,016 to Venkateswar et al. Claims 4 and 5 are finally rejected under 35 USC §103(a) as being unpatentable over Barry et al. and Fujii in further view of U.S. Patent No. 5,946,460 to Hohensee et al.

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[3] *See*, MPEP §2144.03 A. (emphasis added).
[4] *Chevenard*, 139 F.2d at 713, 60 USPQ at 241.
[5] MPEP§2163 ¶III.A ("When appropriate, suggest amendments to the claims which can be supported by the application's written description, being mindful of the prohibition against the addition of new matter in the claims or description. See *Rasmussen*, 650 F.2d at 1214, 211 USPQ at 326.")

Applicant notes at the outset that Venkateswar et al. provides "One embodiment of a sort-first implementation using a **single-chip multiprocessor** is shown in FIG. 2a." col. 5, lines 45 – 46 (emphasis added). Thus, Venkateswar et al. teaches integrating both the master processor and the parallel processors are part of the same chip. Therefore, Venkateswar et al. teaches away[6] from adding and removing image processors, which is evidence of non-obviousness.

Claims 1 and 3

In responding to the applicant's previous remarks with regard to claim 1, that Barry et al. fails to teach "directly connecting the sequencer with the input ports of the raster image processors;" the final Office action asserts that "[t]he instruction operator is considered to be directly connected to the raster image processors because the output provides a physical transmission line to the inputs of the raster image processors." Who considers it so? Certainly not Barry et al. Certainly not Barry et al. Figure 1b. Nor has any reference of record been cited to support this assertion.

The final Office action rationalizes that "[w]hether, the transmission line is routed through the distributor, the wiring still provides a physical path to the raster image processors." Applicants are unable to find the use of "transmission" or "transmission line" anywhere in Barry et al. Nor does the description of the Barry et al. instruction operator 114, distributor block 118, print paths 140/142, 144/146, 148/151, or RIP engines 150, 152, 154 teach or suggest a "transmission line" from the Barry et al. instruction operator 114 to the Barry et al. RIP engines 150, 152, 154.

Instead, as has been previously noted, Barry et al. teaches that "the distributor block 118 is provided to distribute in multiple print job files, … segmented or partitioned

[6] MPEP §2145 X.D.2. (It is improper to combine references where the references teach away from their combination. *In re Grasselli*, 713 F.2d 731, 743, 218 USPQ 769, 779 (Fed. Cir. 1983)).

by instruction operator 114 for processing according to separate processes in a plurality of parallel sections of the print system … ." col. 5, lines 8 – 13. Very clearly, the Barry et al. distributor block 118 functions as more than a "transmission line" as the final Office action asserts. Moreover Barry et al. specifically recites that the distributor "has **several other outputs** including an output … coupled along path 146 from distributor 118 to a second RIP engine 152 … [and] an **nth** select portion 148 is also coupled from distributor 118 … to an **nth** RIP engine 154 representing the last partitioned print job file … separately processed in a parallel path." *Id*, lines 31 – 38 (emphasis added). So, Barry et al. specifically includes separate paths 142, 146 and 151 from the distributor 118 to the RIP engines 142.

Even if one were to concede, *arguendo*, that because the Barry et al. instruction operator 114 interfaces through the Barry et al. distributor 118 to the Barry et al. RIP engines 150, 152, 154, the Barry et al. instruction operator 114 is networked with the Barry et al. RIP engines 150, 152, 154, the result still falls far short. Instead, because of the intervening Barry et al. distributor 118, the output of the Barry et al. instruction operator 114 is not "networked and communicating with, and directly connected to, the input ports of said plurality of raster image processors" as claim 1 recites.

The final Office action further analogizes ignoring the intervening Barry et al. distributor 118 "[i]n the same way, a computer can be considered directly connected to the internet although it may be routed through a modem or a device may be directly connected to a power source even if the power is routed through transistors." Who considers it so? Perhaps someone with no skill in the art, but not someone skilled in the art, with ordinary skill or otherwise. A direct connection is just that, directly connected with no intervening coupling. Even someone connected using a broadband modem is connected through an ISP. If power routed through transistors is "directly connected to a power source," then all circuits are meaningless because, eventually all transistors and all circuit nodes are "directly connected to a power source."

The final Office action concludes that, "since it has been held that omission of an element and its function in a combination where the remaining elements perform the same functions as before involves only routine skill in the art and therefore would have been obvious to one having ordinary skill in the art at the time of the invention." Following this rationale and painting with this same broad brush, Barry et al. was unpatentable over any other printer or even a typewriter. However, Barry et al. was patented. The present invention is different than Barry et al. This is apparent from the present application and Barry et al. Therefore, the present invention is patentable.

Therefore, since claim 1 recites "a sequencer which has an **output port** networked and communicating with, **and directly connected to**, the **input ports** of said plurality of raster image processors" at lines 9 – 11 (emphasis added), not "a sequencer (instruction operator for job file 114 of Fig. 1a) which has an output port networked and communicating with the input ports of said plurality of raster image processors;" since claim 1 is read on Barry et al. and Fujii et al. only by ignoring the Barry et al. distributor block 118 or, by replacing the Barry et al. distributor block 118 with elements that are not found in Barry et al.; the combination of Barry et al. with Fujii et al. fails to result in the present invention as recited in claim 1. Furthermore, since nothing was shown in any of the references that expressly or impliedly suggest the claimed invention as recited in claim 1; since instead, the final Office action very clearly resorts to improper hindsight to replace the Barry et al. distributor block 118 with a transmission line; the present application is being used in improper hindsight to suggest claim 1 and to suggest modifying the references to result in claim 1.

Therefore, *prima facie* obviousness has not been established for claim 1 or any claim depending therefrom. Since claim 3 depends from claim 1, *prima facie* obviousness has not been established for claim 3. Further, because *prima facie* obviousness has not been established and because Venkateswar et al. teaches away from the present invention, claims 1 and 3 are not made obvious by the combination of Barry

et al. with Fujii et al. Reconsideration and withdrawal of the final rejection of claims 1 and 3 under 35 U.S.C. §103(a) is respectfully requested.

Claims 4, 5 and 11

In responding to the applicant's argument "that: Fujii et al. does not teach multiple print head drivers between a print server and a printer," the final Office action asserts that "Barry et al. disclose a pipeline of elements connected between a server (print driver 1020 of Fig 10, col. 15, lines 10 – 28) and a printer (printer 1026 of Fig 10, col. 15, lines 10 – 28)." It is apparent from Barry et al. Fig 10 that 1026 is not a printer, but that the printer is labeled 1018. It is further apparent that the Barry et al. net interface is labeled 1026 and, therefore, "printer 1026" is a typo that should read printer 1018. Therefore, Barry et al. col. 15, lines 10 – 28 provides that

> control PC 1020 is operable to receive requests from the user PC 1008 for information and effect a communication therewith through a TCP/IP interconnection. Once the interconnection is facilitated, the user at the user location 1004 can then request information in the form of all or a portion of certain jobs for output on the display 1012 at the user's location or even on a printer

1018. So, someone can print from PC 1008 to local printer 1018 connected to the PC 1008. This has nothing to do with multiple print head drivers between a print server and a printer.

Nor is there anything in any of this that could be considered a print head driver within the plain meaning in the art, as evidenced by Fujii et al.[7] or within the meaning set forth in the specification[8]. Therefore, very clearly "Fujii et al. does not teach multiple print head drivers between a print server and a printer." Neither, as was previously noted

[7] *See, e.g.*, col. 6, lines 14 – 17 ("A drive voltage pulse signal is applied by head driver 62 between the common electrode 61 and individual electrode 60 of the nozzle to be driven.") and lines 67 – 69 ("A drive voltage pulse is applied appropriately from a head driver 34 to the corresponding ink jet head unit 5 to discharge an ink drop from the ink nozzle.")
[8] *Supra.*

does Barry et al, show or suggest "a pipeline of elements connected between a print server and a printer and processing print control data from said print server," and wherein the pipeline elements are as claim 5 recites. Neither is this shortcoming of the combination of Barry et al. with the Fujii et al. cured by the addition of Hohensee et al. Therefore, nothing has been provided to indicate where it might be found in the cited references that "a pipeline of elements connected between a print server and a printer and processing print control data from said print server," as claim 5 recites. Nor could there be!

Therefore the combination of Barry et al. with Fujii et al. and Hohensee et al. or further in combination with any reference of record, does not result in the present invention as recited in claim 4, 5 or in claim 11, which depends from claim 5. Accordingly, since the combination of Barry et al. with Fujii et al. and Hohensee et al. does not result in the present invention as recited in claims 4 or 5, and because Venkateswar et al. teaches away from the present invention, claims 4 and 5 are not made obvious under 35 U.S.C. §103(a) by Barry et al. with Fujii et al. and Hohensee et al. or further in combination with any reference of record. Reconsideration and withdrawal of the final rejection of claim 5 under 35 U.S.C. §103(a) is respectfully requested.

Claims 6 – 9

The final Office action capsulizes the applicant's prior discussion of what is missing from the references regarding claims 6 – 9, as "Venkateswar et al. '016 does not teach communicating queued packaged print stream data portions directly over a network." In response, the final Office action counters that "Venkateswar et al. discloses queuing packaged print stream data portions; … (col. 2, lines 21-28);" contending that "[t]he network, which may constitute any connection to the raster image processors, can be shown in Fig. 2a as the arrow leading from the master processor to the parallel processors." While that may be so, there must be something in the Venkateswar et al.

written description to indicate that "the arrow leading from the master processor to the parallel processors" truly represents a network.

Instead, Venkateswar et al. provides that "[o]ne embodiment of a sort-first implementation using a **single-chip multiprocessor** is shown in FIG. 2a." col. 5, lines 45 – 46 (emphasis added). Thus both the Venkateswar et al. master processor and the parallel processors are part of the same chip. Very clearly, the arrow from scheduling in the Venkateswar et al. master processor to Boundary Processing Rasterization in the Venkateswar et al. parallel processors is not a network within the plain meaning in the art. To assert otherwise, some extrinsic evidence must be shown to support the assertion that someone with ordinary skill in the art would understand that such an arrow indicated an on-chip network. None has!

Therefore, no reference of record teaches or suggests "communicating queued packaged print stream data portions directly over a network to a plurality of raster image processors" as claim 6 recites. Accordingly, *prima facie* obviousness has not been established for claim 6 or any claim depending therefrom. Nor is the present invention as recited in claims 6 – 9 taught or suggested by any of Barry et al., Fujii et al., Venkateswar et al., or any other reference of record. Therefore, the combination of Barry et al., Fujii et al. and Venkateswar et al. or, further in combination with any other reference of record does not result in the present invention as recited in claim 6 or 9 or, in claim 7 or 8 which depend from claim 6. Reconsideration and withdrawal of the final rejection of claims 6 – 9 under 35 U.S.C. §103(a) is respectfully requested.

Claims 2, 10 and 11

As noted hereinabove, claims 10 and 11 recite that "the sequencer's said output port is connected to the raster image processors' said input ports, and wherein said raster image processors may be connected and disconnected to said sequencer output port, said

sequencer remaining unchanged by additions and removals of connected and disconnected said raster image processors." This is not possible with, nor is it suggested by, any reference of record.

As previously noted, adding another RIP engine to Barry et al., for example, requires adding another line/path. Venkateswar et al. has been offered to teach "a sequencer (main processor 52) being connected to raster image processors (parallel processors 54) (Fig. 2a)." However, as noted hereinabove, Venkateswar et al. FIG. 2a shows a single-chip multiprocessor with the master processor on the same chip as the parallel processors. Clearly, one could not add and subtract processors from such a single chip. Instead, because Venkateswar et al. teaches a single-chip multiprocessor that includes the master processor and parallel processors, Venkateswar et al. teaches away[9] from connecting and disconnecting processor.

Applicants note that "[d]uring patent examination, the pending claims must be 'given *>their< broadest **reasonable** interpretation **consistent with the specification**.' >*In re Hyatt*, 211 F.3d 1367, 1372, 54 USPQ2d 1664, 1667 (Fed. Cir. 2000)[10]." Even if one were to accept arguendo that Venkateswar et al. the main processor 52 were a sequencer within the meaning of the present application, the combination of the Barry et al. distributor 116 in a single chip with the Venkateswar et al. main processor 52 does not change the configuration. Moreover, it does not change the configuration so that "the sequencer's said output port is connected to the raster image processors' said input ports, and wherein said raster image processors **may be connected and disconnected** to said sequencer output port, said sequencer remaining unchanged by additions and removals of connected and disconnected said raster image processors" (emphasis added).

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[9] *Supra*.

[10] MPEP, §2111 (That "broadest reasonable interpretation of the claims **must also be consistent** with the interpretation that those skilled in the art would reach. *In re Cortright*, 165 F.3d 1353, 1359, 49 USPQ2d 1464, 1468 (Fed. Cir. 1999)." (emphasis added)).

Therefore, neither of Barry et al., Fugii et al., Hohensee et al. or Venkateswar et al. teaches or suggests facilely adding or removing raster image processors at the sequencer output port as recited in claims 10 and 11. Moreover Venkateswar et al. teaches away from the combination. Thus, neither does the combination of Barry et al. with Fujii et al., alone or further in combination with any reference of record, suggests or results in the present invention as recited in claims 2, 4, 10 and 11. Nor has the final Office action shown that this recited difference is taught in any reference of record. Because, this difference has not been shown in any reference of record and, further, ignored in rejecting claims 2, 4, 10 and 11 and, because so Venkateswar et al. teaches away from the combination, *prima facie* obviousness has not been established for either of claims 2, 4, 10 or 11. Reconsideration and withdrawal of the final rejection of claims 2, 4, 10 and 11 under 35 U.S.C. §103(a) is respectfully requested.

Conclusion

The applicants thank the Examiner for efforts, both past and present, in examining the application. Believing the application to be in condition for allowance for the reasons set forth above, the applicants respectfully request that the Examiner reconsider and withdraw the final rejection of claims 1 – 11 under 35 U.S.C. §§101, 103(a) and 112, and allow the application to issue.

As previously noted the MPEP §706 "Rejection of Claims," subsection III, "PATENTABLE SUBJECT MATTER DISCLOSED BUT NOT CLAIMED" provides in pertinent part that

> If **the examiner** is satisfied after the search has been completed that patentable subject matter has been disclosed and the record indicates that the applicant intends to claim such subject matter, he or she **may note** in the Office action that **certain aspects or features** of the patentable invention have not been claimed and that if properly claimed such claims **may be given favorable consideration**. (emphasis added.)

The applicants believe that the written description of the present application is quite different than, and not suggested by, any reference of record. Accordingly, should the Examiner believe anything further may be required, the Examiner is requested to contact the undersigned attorney at the local telephone number listed below for a telephonic or personal interview to discuss any other changes.

Please charge any deficiencies in fees and credit any overpayment of fees to IBM Corporation Deposit Account No. 50-3669 and advise us accordingly.

Respectfully Submitted,

July 19, 2007
(Date)

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